CLAIMS

What is claimed is:

1. A device age determination circuit comprising:

a first circuit for operating at a first duty cycle and for generating a first output;

a second circuit for operating at a second duty cycle different from said first duty cycle and for generating a second output; and

a measuring circuit for determining a difference between said first output and said second output, said difference indicating an age of said device.

2. The circuit as recited in Claim 1 wherein said first circuit and said second circuit are analogous circuits.

3. The circuit as recited in Claim 1 wherein said first circuit and said second circuit are ring oscillator circuits.

4. The circuit as recited in Claim 3 wherein said ring oscillator circuits are nineteen stage ring oscillator circuits.

5. The circuit as recited in Claim 3 wherein said ring oscillator circuits comprise an enable switch.

6. The circuit as recited in Claim 1 wherein said first duty cycle is substantially normally on and said second duty cycle is substantially normally off.

7. The circuit as recited in Claim 6 wherein said second circuit is powered down.

8. The circuit as recited in Claim 6 wherein said second circuit is powered up but not enabled.

9. The circuit as recited in Claim 6 wherein said first circuit is powered up in response to a powergood signal.

10. The circuit as recited in Claim 6 wherein said first circuit is powered up in response to a resetb signal.

11. The circuit as recited in Claim 1 wherein said device is an integrated circuit.

12. The circuit as recited in Claim 1 wherein said measuring circuit comprises:

a multiplexer for selecting between said first output and said second output; and

a counter circuit for receiving said first output and said second output, and for determining said difference.

13. The circuit as recited in Claim 12 wherein said measuring circuit further comprises at least one frequency divider circuit for standardizing said first output and said second output.

14. The circuit as recited in Claim 1 wherein said measuring circuit comprises:

a first counter circuit for receiving said first output; and

a second counter circuit for receiving said second output.

15. The circuit as recited in Claim 14 wherein said measuring circuit further comprises:

a first frequency divider circuit for standardizing said first output; and

a second frequency divider circuit for standardizing said second output.

16. The circuit as recited in Claim 1 wherein said first output is measured at a node of said first circuit and wherein said second output is measured at a node of said second circuit.

17. The circuit as recited in Claim 3 wherein said first output is a first frequency and said second output is a second frequency.

18. The circuit as recited in Claim 1 wherein said measuring circuit is operable to compensate for an initial offset in determining said difference.

19. A device age determination circuit comprising:

a first oscillator circuit for operating at a first duty cycle and for generating a first frequency, wherein said first duty cycle is substantially normally on;

a second oscillator circuit for operating at a second duty cycle different from said first duty cycle and for generating a second frequency, wherein said second duty cycle is substantially normally off; and

a measuring circuit for determining a difference between said first frequency and said second frequency, said difference indicating an age of said device.

20. The circuit as recited in Claim 19 wherein said first oscillator circuit and said second oscillator circuit are analogous oscillator circuits.

21. The circuit as recited in Claim 19 wherein said first oscillator circuit and said second oscillator circuit are ring oscillator circuits.

22. The circuit as recited in Claim 19 wherein said first oscillator circuit comprises a first enable switch and said second oscillator circuit comprises a second enable switch.

23. The circuit as recited in Claim 19 wherein said second oscillator circuit is powered down.

24. The circuit as recited in Claim 19 wherein said second oscillator circuit is powered up but not enabled.

25. The circuit as recited in Claim 19 wherein said first oscillator circuit is powered up in response to a powergood signal.

26. The circuit as recited in Claim 19 wherein said first oscillator circuit is powered up in response to a resetb signal.

27. The circuit as recited in Claim 19 wherein said device is an integrated circuit.

28. The circuit as recited in Claim 19 wherein said measuring circuit comprises:

a multiplexer for selecting between said first frequency and said second frequency; and

a counter circuit for receiving said first frequency and said second frequency, and for determining said difference.

29. The circuit as recited in Claim 28 wherein said measuring circuit further comprises at least one frequency divider circuit for standardizing said first frequency and said second frequency.

30. The circuit as recited in Claim 19 wherein said measuring circuit comprises:

a first counter circuit for receiving said first frequency; and

a second counter circuit for receiving said second frequency.

31. The circuit as recited in Claim 30 wherein said measuring circuit further comprises:

a first frequency divider circuit for standardizing said first frequency; and

a second frequency divider circuit for standardizing said second frequency.

32. The circuit as recited in Claim 19 wherein said first frequency is measured at a node of said first oscillator circuit and wherein said second frequency is measured at a node of said second oscillator circuit.

33. The circuit as recited in Claim 19 wherein said measuring circuit is operable to compensate for an initial offset in determining said difference.

34. A method for determining an age of a device, said method comprising:

receiving a first output from a first circuit operating at a first duty cycle;

receiving a second output from a second circuit operating at second duty cycle different from said first duty cycle; and

determining a difference between said first output and said second output, said difference indicating an age of said device.

35. The method as recited in Claim 34 wherein said first circuit and said second circuit are analogous circuits.

36. The method as recited in Claim 34 wherein said first circuit and said second circuit are ring oscillator circuits.

37. The method as recited in Claim 36 wherein said ring oscillator circuits are nineteen stage ring oscillator circuits.

38. The method as recited in Claim 36 wherein said ring oscillator circuits comprise an enable switch.

39. The method as recited in Claim 34 wherein said first duty cycle is substantially normally on and said second duty cycle is substantially normally off.

40. The method as recited in Claim 39 wherein said second circuit is powered down.

41. The method as recited in Claim 39 wherein said second circuit is powered up but not enabled.

42. The method as recited in Claim 39 wherein said first circuit is powered up in response to a powergood signal.

43. The method as recited in Claim 39 wherein said first circuit is powered up in response to a resetb signal.

44. The method as recited in Claim 34 wherein said device is an integrated circuit.

45. The method as recited in Claim 34 wherein said determining comprises dividing said first output and said second output in order to standardize said first output and said second output.

46. The method as recited in Claim 34 wherein said first output is measured at a node of said first circuit and wherein said second output is measured at a node of said second circuit.

47. The method as recited in Claim 34 wherein said first output is a first frequency and said second output is a second frequency.

48. The method as recited in Claim 34 wherein said determining comprises by compensating for an initial offset of the first output and the second output.